SPECIFICATION AMENDMENTS

Please replace paragraph [0001] of the specification with the following amended paragraph:

[0001] This application is related to Scheuerlein et al., US Application No. [[_____]] 10/728,451, "High Density Contact to Relaxed Geometry Layers," ~~(attorney docket no. MA-112)~~ filed on even date herewith, which application is hereby incorporated by reference.

Please replace paragraph [0059] of the specification with the following amended paragraph:

[0059] An alternating phase shift mask paired with a quadrupole aperture is highly effective for patterning regularly spaced pillars. A novel alternating phase shift mask useful for patterning regularly spaced pillars is disclosed in Chen, US Patent Application No. [[_____]] 10/728,436, filed on even date herewith ~~(attorney docket no. MA-111)~~ and hereby incorporated by reference.

Please replace paragraph [0074] of the specification with the following amended paragraph:

[0074] Still other space-saving techniques that can profitably be used to further reduce required substrate area for connections to support circuitry are described in the related Scheuerlein application ~~(atty docket no. MA-112)~~ recited in the first paragraph of the present application and filed on even date herewith. This application teaches a via and staggered routing level structure. Vertically overlapping vias connect to two or more routing levels formed at different heights. The routing levels are either both formed above or both formed below the vias, and all are formed above a semiconductor substrate wafer. In this way vias can be formed having a pitch smaller than the pitch of either the first routing level or the second routing level, saving space. An illustrative embodiment that could advantageously be used in the present invention is shown in Fig. 3 of

PAGE 7/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46

[[_____]] 10/728,451, the Scheuerlein application filed on even date herewith ~~(MA-112.)~~.

Please add the following new paragraphs [0072.1]-[0072.5] between paragraphs [0072] and [0073]:

[0072.1] Referring now to Fig. 12, a schematic diagram is depicted which represents a memory plane within an exemplary three-dimensional passive element memory array. One such memory plane 150 is shown, although preferably other memory planes are similarly arranged, as described in greater detail herebelow. The memory plane 150 includes a plurality of blocks, such as blocks 151, 152, and 153. Each block includes a plurality of word lines, such as word lines 156 associated with block 152. Each block also includes a plurality of bit line segments, such as bit line segments 157, 158, 159, and 160 associated with block 152. As indicated, a memory cell (e.g., memory cell 173) is formed between each word line and each bit line segment within a block.

[0072.2] Each bit line segment may be coupled to an associated global bit line by a segment switch device which is controlled by a block select signal. For example, bit line segment 157 is coupled by a segment switch device 161 to global bit line 154, which preferably resides on a different layer of the memory array. The connection path to the global bit line is formed by way of a vertical connection 167, which is shared by other memory planes, to provide a path for a bit line segment from any of at least two memory planes to be coupled to the global bit line.

[0072.3] The bit line segments of memory plane 150 are arranged in a 2:1 interleaved configuration, which allows the required pitch of the global bit lines to be twice that of the bit line segments. In this particular interleave arrangement half of the bit line segments within a block exit to the top of the block and are coupled under control of a SELECT-A control signal to the respective global bit lines, while the other half of the bit line segments exit to the bottom of the block and are coupled under control of a SELECT-B control signal to the same respective global bit lines. In particular, bit line segment 158 is coupled by segment switch device 163 to a shared vertical connection 169

PAGE 8/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46

to global bit line 154, bit line segment 159 is coupled by segment switch device 162 to a shared vertical connection 168 to global bit line 155, and bit line segment 160 is coupled by segment switch device 164 to a shared vertical connection 170 to global bit line 155.

[0072.4] In this exemplary configuration each of the shared vertical connections (which are shared vertically with other memory planes) is also shared by a bit line segment in an adjacent memory block within the same memory plane. For example, a bit line segment in block 151 (unlabeled) is coupled by segment switch device 171 (under control of a block select signal SELECT-E) to the same shared vertical connection 167, and consequently to global bit line 154. In other words, a bit line segment from each of two adjacent blocks shares a vertical connection to an associated global bit line, to achieve a global bit line pitch that is twice the pitch of the bit line segments. In particular another bit line segment in block 151 (unlabeled) is coupled by segment switch device 172 (controlled by SELECT-E) to the shared vertical connection 168, and consequently to global bit line 155. As described below, other interleave arrangements are also contemplated. Likewise bit line segments from memory block 153 are respectively coupled by segment switch devices 165, 166 to shared vertical connections 169, 170 and consequently to global bit lines 154, 155.

[0072.5] In this embodiment each global bit line is operably coupled to a respective bit line segment in a selected block of a selected memory plane by driving one of the two block select control signals associated with the selected block to an active state, while leaving the other block select control signal of the selected block, and all other blocks (both on the same memory plane and on other memory planes sharing the same global bit lines), at an inactive level. In a read operation, the signal from a memory cell is coupled from the bit line segment to a global bit line, and subsequently to sensing circuitry. In a write operation, the programming voltages and currents are conveyed from write driver circuitry, through the global bit line, through the segment switch device to the bit line segment, and coupled thereby to the selected memory cell.

PAGE 9/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46

Please add the following new paragraphs [0070.1]-[0070.6] between paragraphs [0070] and [0071]:

[0070.1] Referring now to Fig. 13, an electrical schematic is shown of a portion of an exemplary memory array. The portion shown may represent a two-dimensional array having only one plane of memory cells, or may represent one level of three-dimensional memory array having more than one level (i.e., more than one plane) of memory cells. A plurality of series-connected NAND transistor strings is shown, one of which is labeled 122. Each string includes a plurality of SONOS transistors connected in series, each gated by a respective one of a plurality of word lines 125. The NAND string 122 also includes a block select device 148 for coupling one end of the NAND string to a global bit line contact 131 in accordance with a block select signal BSEL2 conveyed on node 126, and further includes a second block select device 147 for coupling the other end of the NAND string to a shared bias node 128 in accordance with a block select signal BSEL1 conveyed on node 124. The global bit line contact 131 is shared with another NAND string 132 which is disposed on the other side of (i.e., opposite) the global bit line contact 131 and is independently selectable by another block select signal BSEL3.

[0070.2] As is depicted in the figure, a group of four laterally adjacent NAND strings share a common bias node 128, which may be termed VDRAIN1, disposed at the left end of the NAND strings, but are individually coupled to a respective one of four global bit line contacts disposed at the right end of the NAND string. The next group of four laterally adjacent NAND strings is reversed, and the NAND strings in the group are individually coupled to a respective one of four global bit line contacts disposed at the left end of the NAND strings. This next group of NAND strings shares a common bias node 129, which may be termed VDRAIN2, disposed at the right end of the NAND strings. As may be appreciated, the block select signal BSEL1 couples the left end of half of the NAND strings to an associated global bit line, while the same signal couples the right end of the other half of the NAND strings to the shared bias node VDRAIN1. Similarly, block select signal BSEL2 couples the right end of half of the NAND strings to an associated global bit line, while the same signal couples the right end of the other half of the NAND strings to the shared bias node VDRAIN2.

PAGE 10/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46

[0070.3] This structure interleaves the NAND strings by coupling two different NAND strings to the same global bit line. For example, the left end of NAND string 134 is coupled by BSEL1 to a global bit line contact 138, while the right end of NAND string 136 is coupled by BSEL2 to a global bit line contact 140. These two global bit line contacts 138 and 140 are preferably connected to the same global bit line, which may be routed horizontally on a wire 146 conveyed on a different wiring level. Such global bit lines may be conveyed a wiring level below the array, or alternatively above the array, or alternatively on a wiring level within the array (e.g., in a three-dimensional array having more than one level). The NAND string 134 and 136 may be referred to as "adjacent" NAND strings, as sharing the same global bit line and sharing the same word lines (i.e., within the same block of the array), even though there is another NAND string disposed between them. It is still possible to select only one of these two NAND strings for reading and writing because the shared bias nodes VDRAIN1 and VDRAIN2 are distinct and may be driven to different conditions, as is described in regards to the next several figures. Each of these two shared bias nodes VDRAIN1 and VDRAIN2 is shared by NAND strings in two adjacent blocks, and thus are preferably conveyed in vertical wires 142 and 144, respectively, which are preferably conveyed on a wiring level "above" the memory array (i.e., further from the semiconductor substrate). Consequently, the two shared bias nodes VDRAIN1 and VDRAIN2, the block select signals BSEL1 and BSEL2, and the various word lines 125, which all traverse across the memory array in the same direction, may be more conveniently decoded and driven to appropriate levels.

[0070.4] As described above, the memory cells in the NAND strings (i.e., those gated by one of the word lines) are preferably SONOS structures. As used herein, the term SONOS is meant to refer to the general class of transistor devices having a charge storage dielectric layer between the gate and the underlying channel, and is not used in a restrictive sense to merely imply a literal silicon-oxide-nitride-oxide-silicon layer stack. For example, other kinds of dielectric layers may be employed, such as oxynitrides, as is described in greater detail herebelow.

PAGE 11/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46

[0070.5] A basic NAND string is a very efficient structure, capable of achieving a $4F^2$ layout for the incremental transistor memory cell. However, providing the necessary switch devices with appropriate control signals at the ends of the NAND strings, and the overhead of connecting such NAND strings to global bit lines and to bias or ground nodes, frequently degrades the resultant total efficiency. In contrast, the structure depicted in Fig. 13 achieves very dense layout because of the interleaving of two NAND strings, both coupled to the same global bit line, thus relaxing the pitch requirements for the global bit lines by a factor of two. The structure depicted in Fig. 13 also achieves very dense layout because only one control signal is utilized at each end of the NAND strings. This allows the two block select lines BSEL1 and BSEL2 to route in continuous polysilicon stripes across the plurality of channel stripes, just like the word lines, without any provision being otherwise required for contacting a block select signal line to some but not all of the block select transistors formed in the channel stripes.

[0070.6] Another factor contributing to the efficiency of this array structure is the ability of the block select devices to be fabricated identically to the memory cell devices. In other words, the block select devices may be SONOS devices just like the memory cell devices. In 3D array embodiments having more than one memory level formed above a semiconductor substrate, each memory level consequently includes only one type of device, further simplifying the fabrication of each level. The block select devices may be sized identically to the memory cell devices, but preferably may have a longer channel length (i.e., wider polysilicon stripe for the block select signals) to increase the breakdown voltage of the block select devices.

Please add new paragraph [0037.1] between paragraphs [0037] and [0038]:

[0075] Fig. 11 illustrates a semiconductor die comprising: a substrate device level L1 having a substrate pitch P1; and a first above-substrate device level L2 formed above the substrate device level L1, the first above-substrate device level having a first above-substrate pitch P2, wherein the first above-substrate pitch P2 is smaller than the substrate pitch P1. A second above-substrate device level L3 is formed over the first above-substrate device level L2, the second above-substrate device level L3 having a second

PAGE 12/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46

above-substrate pitch P3, wherein the second above-substrate pitch P3 is smaller than the substrate pitch P1.

PAGE 13/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46

SPECIFICATION AMENDMENTS: DISCUSSION

The Examiner required that the specification be amended to supply the missing application number in paragraph [0001], which was not available at the time of filing. A replacement paragraph, including the correct application number, is provided, with markups showing changes made.

Similar corrections are made in paragraphs [0059] and [0074] where application numbers were also unavailable at the time of filing. Replacement paragraphs are provided with markups showing changes made.

New paragraphs [0072.1]-[0072.5] have been added between paragraphs [0072] and [0073]. These paragraphs are drawn from United States Patent Application No. 10/403752, which was incorporated by reference at paragraph [0072], and thus do not constitute new matter.

New paragraphs [0070.1]-[0070.6] have been added between paragraphs [0070] and [0071]. These paragraphs are drawn from Scheuerlein et al., US Patent Application No. 10/335078, which was incorporated by reference at paragraph [0030], and thus do not constitute new matter.

New paragraph [0037.1] is added between paragraphs [0037] and [0038]. This paragraph refers to elements of new Fig. 11. It is a restatement of the subject matter of paragraphs [0006]-[0011], [0032]-[0034], and [0037]-[0040], and thus does not constitute new matter.

PAGE 14/27 * RCVD AT 5/24/2006 2:51:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/10 * DNIS:2738300 * CSID:408 969 4849 * DURATION (mm-ss):08-46